# I2C programming notes

## Clock requirements

The I2C kernel is clocked by I2CCLK. The Period TI2CCLK must respect the following conditions:

TI2CCLK < (tLOW – tFilters) / 4 AND tICCLK < tHIGH

tLOW: SCL low time tHIGH: SCL high time

tFilters: sum of delays brought by the filters. Analog filters delay is maximum 260ns.

Digital filter delay is DNF\* TI2CCLK

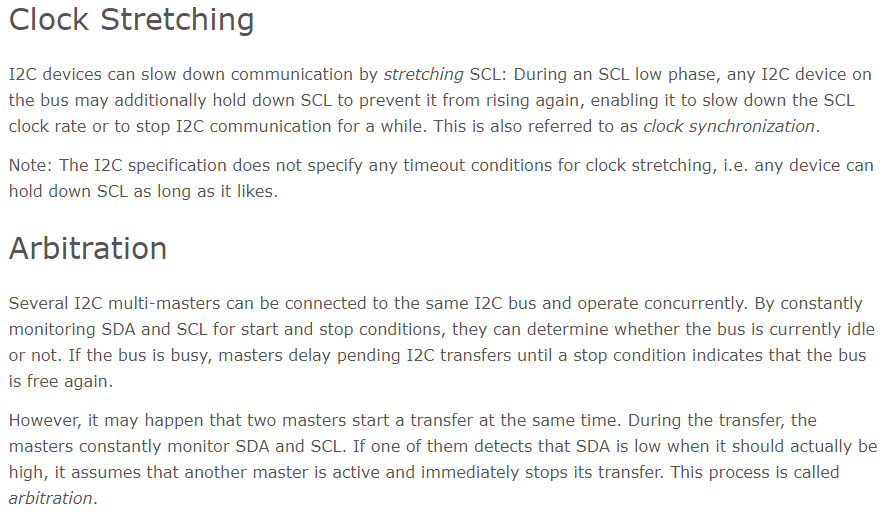
The PCLK period tPCLK must respect the following conditions:

TPCLK < 4/3 TSCL

If the I2C kernel is clocked by PCLK. PCLK must respect the conditions for IC2CLK

## Mode Selection

By default set to slave mode. Select Master transmitter mode. The interface automatically switches from slave to master when it generates a START condition, and from master to slave if an arbitration loss or a STOP generation occurs, allowing multimaster capability.



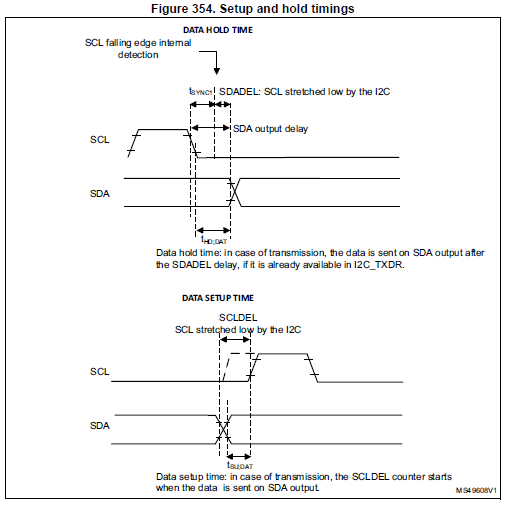
<https://www.i2c-bus.org/i2c-primer/clock-generation-stretching-arbitration/>

## Noise Filters

By default an analog Filter is present on the SDA and SCL inputs which suppresses spikes with a pulls width up to 50ns. Analog filter can be disabled by setting ANFOFF bit in the I2C\_CR1 register.

Digital filter can be enabled by configuring DNF in the I2C\_CR1 register. Digital filter will stop the SDA and SCL lines form changing value unless it remains stable for a programmable length of DNF\*I2CCLK.

## Timings



The timings must be configured in order to guarantee a correct data hold and setup time, used in master and slave modes.

This is done by programming the PRESC[3:0], SCLDEL[3:0] and SDADEL[3:0] bits in the I2C\_TIMINGR register.

The STM32CubeMX tool calculates and provides the I2C\_TIMINGR content in the I2C

### SDADEL and PRESC

When the SCL falling edge is internally detected, a delay is inserted before sending SDA output. This delay is: tSDADEL = SDADEL x tPRESC + tI2CCLK where tPRESC = (PRESC+1) x tI2CCLK.

The total SDA output delay is: tSYNC1 + {[SDADEL x (PRESC+1) + 1] x tI2CCLK }

tSYNC1 duration depends on these parameters:

– SCL falling slope

– When enabled, input delay brought by the analog filter: tAF(min) < tAF < tAF(max)

– When enabled, input delay brought by the digital filter: tDNF = DNF x tI2CCLK

– Delay due to SCL synchronization to I2CCLK clock (2 to 3 I2CCLK periods)

In order to bridge the undefined region of the SCL falling edge, the user must program

SDADEL in such a way that:

{ tf (max) + tHD;DAT (min) - tAF(min) - [(*DNF* +3) x tI2CCLK]} / {(PRESC +1) x tI2CCLK } ≤ SDADEL

SDADEL ≤ {tHD;DAT (max) -tAF(max) - [(*DNF+4) x tI2CCLK*]} / {(PRESC +1) x tI2CCLK }

*Note: This condition can be violated when NOSTRETCH=0, because the device stretches SCL*

*low to guarantee the set-up time, according to the SCLDEL value.*

### SCLDEL and PRESC

After tSDADEL delay, or after sending SDA output in case the slave had to stretch the clock because the data was not yet written in I2C\_TXDR register, SCL line is kept at low level during the setup time. This setup time is tSCLDEL = (SCLDEL+1) x tPRESC where tPRESC = (PRESC+1) x tI2CCLK.

In order to bridge the undefined region of the SDA transition (rising edge usually worst

case), the user must program SCLDEL in such a way that:

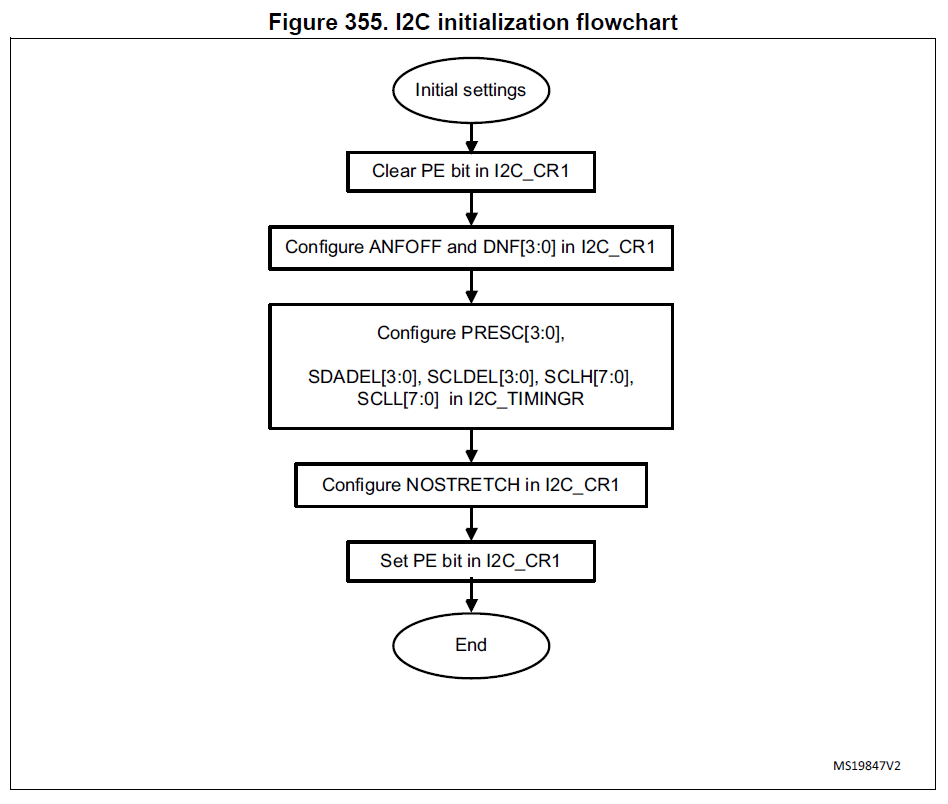
{[tr (max) + tSU;DAT (min)] / [(PRESC+1)] x tI2CCLK]} - 1 <= SCLDEL

The SDA and SCL transition time values to be used are the ones in the application. Using

the maximum values from the standard increases the constraints for the SDADEL and

SCLDEL calculation, but ensures the feature whatever the application.

## Initialization flowchart



## Master initialization

Additionally, in master mode, the SCL clock high and low levels must be configured by programming the PRESC[3:0], SCLH[7:0] and SCLL[7:0] bits in the I2C\_TIMINGR register.

The I2C detects its own SCL low level after a tSYNC1 delay depending on the SCL falling

edge, SCL input noise filters (analog + digital) and SCL synchronization to the I2CxCLK

clock. The I2C releases SCL to high level once the SCLL counter reaches the value

programmed in the SCLL[7:0] bits in the I2C\_TIMINGR register.

When the SCL falling edge is internally detected, a delay is inserted before releasing

the SCL output. This delay is:

tSCLL = (SCLL+1) x tPRESC where tPRESC = (PRESC+1) x tI2CCLK.

tSCLL impacts the SCL low time tLOW .

The I2C detects its own SCL high level after a tSYNC2 delay depending on the SCL rising

edge, SCL input noise filters (analog + digital) and SCL synchronization to I2CxCLK clock.

The I2C ties SCL to low level once the SCLH counter is reached reaches the value

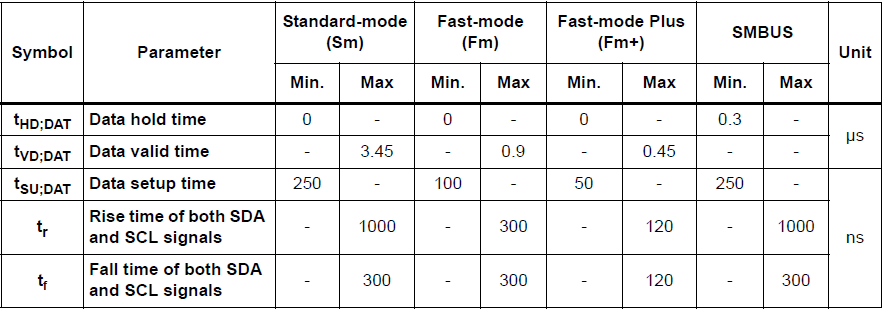
programmed in the SCLH[7:0] bits in the I2C\_TIMINGR register.

When the SCL rising edge is internally detected, a delay is inserted before forcing the

SCL output to low level. This delay is:

tSCLH = (SCLH+1) x tPRESC where tPRESC =(PRESC+1) x tI2CCLK.

tSCLH impacts the SCL high time tHIGH .



Consequently the master clock period is:

tSCL = tSYNC1 + tSYNC2 + {[(SCLH+1) + (SCLL+1)] x (PRESC+1) x tI2CCLK}

= tSYNC1 + tSYNC2 + tSCLL + tSCLH

The duration of tSYNC1 depends on these parameters:

– SCL falling slope

– When enabled, input delay induced by the analog filter.

– When enabled, input delay induced by the digital filter: DNF x tI2CCLK

– Delay due to SCL synchronization with I2CCLK clock (2 to 3 I2CCLK periods)

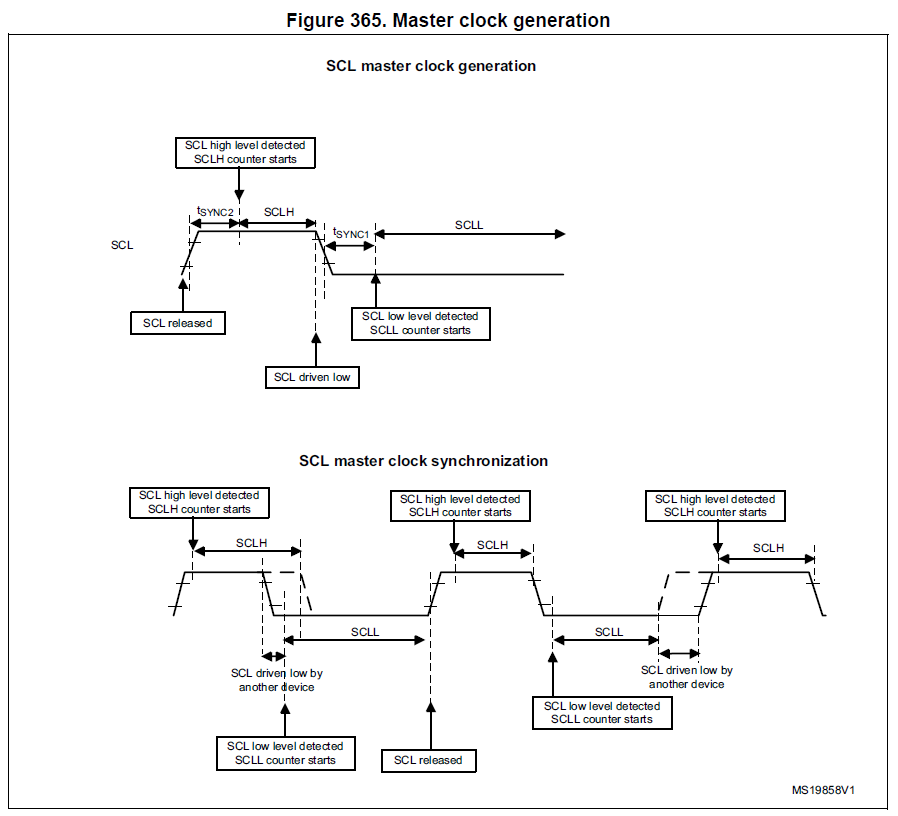
The duration of tSYNC2 depends on these parameters:

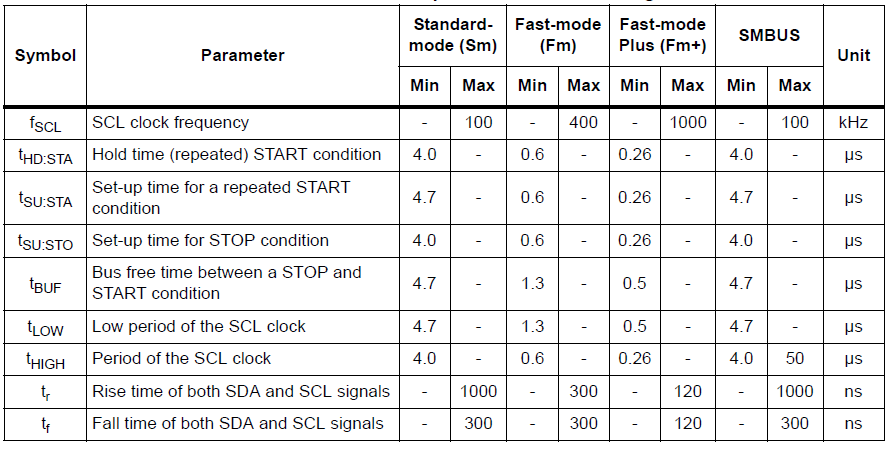
– SCL rising slope

– When enabled, input delay induced by the analog filter.

– When enabled, input delay induced by the digital filter: DNF x tI2CCLK

– Delay due to SCL synchronization with I2CCLK clock (2 to 3 I2CCLK periods)





## Master communication initialization (address phase)

In order to initiate the communication, the user must program the following parameters for

the addressed slave in the I2C\_CR2 register:

* Addressing mode (7-bit or 10-bit): ADD10
* Slave address to be sent: SADD[9:0]
* Transfer direction: RD\_WRN
* In case of 10-bit address read: HEAD10R bit. HEAD10R must be configure to indicate

if the complete address sequence must be sent, or only the header in case of a

direction change.

* The number of bytes to be transferred: NBYTES[7:0]. If the number of bytes is equal to

or greater than 255 bytes, NBYTES[7:0] must initially be filled with 0xFF.

The user must then set the START bit in I2C\_CR2 register. Changing all the above bits is

not allowed when START bit is set.

Then the master automatically sends the START condition followed by the slave address as

soon as it detects that the bus is free (BUSY = 0) and after a delay of tBUF.

In case of an arbitration loss, the master automatically switches back to slave mode and can

acknowledge its own address if it is addressed as a slave.

*Note: The START bit is reset by hardware when the slave address has been sent on the bus,*

*whatever the received acknowledge value. The START bit is also reset by hardware if an*

*arbitration loss occurs. If the I2C is addressed as a slave (ADDR=1) while the START bit is set, the I2C switches to slave mode and the START bit is cleared, when the ADDRCF bit is set.*